Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 41, 43, and 63, as follows:

Listing of Claims:

1. (Previously presented) A clock synchronization circuit adapted to receive an input clock signal and adapted to receive current data signals and respective future data signals, the clock synchronization circuit operable to generate a phase shifted clock signal in response to the input clock signal with the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and respective future data signals.

2. (Previously presented) The clock synchronization circuit of claim 1 wherein the clock synchronization circuit is operable to add a first phase shift increment to the phase shifted clock signal for each pair of current and respective future data signals having the same logic state, and is operable to add a second phase shift increment to the phase shifted clock signal for each pair of current and respective future data signals having complementary logic states.

3. (Original) The clock synchronization circuit of claim 2 wherein the first phase shift increment is greater than the second phase shift increment.

4. (Previously presented) The clock synchronization circuit of claim 1 wherein the phase shift of the phase shifted clock signal comprises a phase shift having a value that is a function of the logic states of the current and future data signals.

5. (Previously presented) The clock synchronization circuit of claim 1 comprising:

a logic circuit coupled to receive the future data and current data signals, and operable to develop a plurality of phase shift control signals in response to the future data and current data signals; and

a phase shift circuit adapted to receive the input clock signal and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate the phase shifted clock signal responsive to the input clock signal, the phase shifted clock signal having a delay determined by the plurality of phase shift control signals.

6. (Previously presented) The clock synchronization circuit of claim 5 wherein the logic circuit comprises a plurality of XNOR gates, each XNOR gate receiving a respective future data signal and the corresponding current data signal and developing a corresponding one of the plurality of phase shift control signal responsive to the future data and current data signals.

7. (Previously presented) The clock synchronization circuit of claim 5 wherein the phase shift circuit comprises:

a plurality of switching circuits coupled to an output node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the respective one of the phase shift control signal having a first state to couple a first phase shift element to the output node and operable responsive to the respective one of the phase shift control signal having a second state to couple a second phase shift element to the output node;

an input circuit having an input adapted to receive the input clock signal and having an output coupled to the output node, and being operable to develop a charging signal on the output node responsive to the input clock signal, the charging signal having a delay in reaching a threshold value that is determined by the first and second phase shift elements coupled to the output node; and

an output circuit coupled to the output node and operable to develop the phase shifted clock signal responsive to the charging signal reaching the threshold value.

8. (Original) The clock synchronization circuit of claim 7 wherein the input and output circuits each comprise an inverter.

9. (Original) The clock synchronization circuit of claim 7 wherein each first phase shift element comprises a first capacitor having a first capacitance and each second phase shift element comprises a second capacitor having a second capacitance, the first capacitance being greater than the second capacitance.

10. (Previously presented) The clock synchronization circuit of claim 9 wherein each of the plurality of switching circuits comprises a first transistor coupled in series with the corresponding first capacitor between the output node and a reference voltage source, and further comprises a second transistor coupled in series with the corresponding second capacitor between the output node and the reference voltage source, each transistor having a control terminal coupled to receive the corresponding phase shift control signal.

11. (Original) The clock synchronization circuit of claim 10 wherein the first transistor comprises an NMOS transistor and the second transistor comprises a PMOS transistor.

12. (Withdrawn) The clock synchronization circuit of claim 5 wherein the phase shift circuit comprises:

an input circuit adapted to receive the input clock signal and being operable to develop an output signal on an output responsive to the input clock signal;

an output circuit having an input coupled to a charging node and being operable to develop the phase shifted clock signal responsive to a charging signal on the charging node reaching a threshold value; and

a plurality of switching circuits coupled in series between the output of the input circuit and the charging node; each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the phase shift control signal having a first state to provide a first phase shift element and operable responsive to

the phase shift control signal having a second state to provide a second phase shift element, the combination of first and second phase shift elements coupled in series controlling a rate at which the charging signal reaches the threshold value.

13. (Withdrawn) The clock synchronization circuit of claim 12 wherein the input and output circuits each comprise an inverter.

14. (Withdrawn) The clock synchronization circuit of claim 12 wherein each first phase shift element comprises a resistor and each second phase shift element comprises a transistor having signal terminals coupled in parallel with the corresponding resistor and having a control terminal coupled to receive the corresponding phase shift control signal.

15. (Withdrawn) The clock synchronization circuit of claim 14 wherein each transistor comprises a NMOS transistor.

16. (Withdrawn) The clock synchronization circuit of claim 5 wherein the delay circuit comprises:

an input circuit adapted to receive the input clock signal and including a supply node, the input circuit operable to develop the phase shifted clock signal responsive to the input clock signal, the phase shift of the phase shifted clock signal being a function of a supply current provided to the supply node; and

a plurality of switching circuits coupled in parallel between a supply voltage source and the supply node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the phase shift control signal having a first state to provide a first current to the supply node and operable responsive to the phase shift control signal having a second state to provide a second current to the supply node, the combination of first and second currents from the plurality of switching circuits controlling the supply current provided to the supply node.

17. (Withdrawn) The clock synchronization circuit of claim 16 wherein each switching circuit comprises a transistor having signal terminals coupled between the supply voltage source and the supply node, and having a control terminal coupled to receive the corresponding delay control signal.

18. (Withdrawn) The clock synchronization circuit of claim 17 wherein each transistor comprises a PMOS transistor.

19. (Withdrawn) The clock synchronization circuit of claim 16 wherein the input circuit comprises a first inverter coupled to receive the input clock signal and including the supply node, and a second inverter coupled in series with the first inverter and operable to develop the delayed clock signal responsive to an output signal from first inverter.

20. (Previously presented) The clock synchronization circuit of claim 1 wherein the phase shift of the phase shifted clock signal comprises a delay relative to the input clock signal.

21. (Previously presented) A data output circuit, comprising:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as a corresponding output data signal; and

a clock synchronization circuit adapted to receive an input clock signal and adapted to receive the respective read and corresponding output data signals, and coupled to the plurality of data drivers, the clock synchronization circuit operable to generate a phase shifted clock signal in response to the input clock signal and apply the phase shifted clock signal to clock the respective read data signals out of the plurality of data drivers as the corresponding output data signals, the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the respective read data and corresponding output data signals.

22. (Previously presented) The data output circuit of claim 21 wherein the clock synchronization circuit is operable to add a first phase shift increment to the phase shift of the phase shifted clock signal for each read data signal and corresponding output data signal having the same logic state, and is operable to alternatively add a second phase shift increment to the phase shift of the phase shifted clock signal for each read data signal and corresponding output data signal having complementary logic states.

23. (Original) The data output circuit of claim 22 wherein the first phase shift increment is greater than the second phase shift increment.

24. (Original) The data output circuit of claim 21 wherein the phase shift of the phase shifted clock signal comprises a phase shift having a value that is a function of the logic states of the read data and output data signals.

25. (Previously presented) A data output circuit, comprising:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as a corresponding output data signal;

a logic circuit coupled to receive the respective read data and the corresponding output data signals, and operable to develop a plurality of phase shift control signals in response to the respective read data and the corresponding output data signals; and

a phase shift circuit adapted to receive an input clock signal and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate the phase shifted clock signal responsive to the input clock signal, the phase shifted clock signal having a phase shift determined by the plurality of phase shift control signals.

26. (Previously presented) The data output circuit of claim 25 wherein the logic circuit comprises a plurality of XNOR gates, each XNOR gate receiving one of the

respective read data and corresponding output data signals and developing a corresponding one of the plurality of phase shift control signals responsive to the one of the respective read data and corresponding output data signals.

27. (Previously presented) The data output circuit of claim 25 wherein the phase shift circuit comprises:

a plurality of switching circuits coupled to an output node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the respective one of the phase shift control signal having a first state to couple a respective first delay element to the output node and operable responsive to the respective one of the phase shift control signals having a second state to couple a respective second delay element to the output node;

an input circuit having an input adapted to receive the input clock signal and having an output coupled to the output node, and being operable to develop a charging signal on the output node responsive to the input clock signal, the charging signal having a delay in reaching a threshold value that is determined by the first and second delay elements coupled to the output node; and

an output circuit coupled to the output node and operable to develop the phase shift clock signal responsive to the charging signal reaching the threshold value.

28. (Original) The data output circuit of claim 27 wherein the input and output circuits each comprise an inverter.

29. (Original) The data output circuit of claim 27 wherein each first delay element comprises a first capacitor having a first capacitance and each second delay element comprises a second capacitor having a second capacitance, the first capacitance being greater than the second capacitance.

30. (Previously presented) The data output circuit of claim 29 wherein each switching circuit comprises a first transistor coupled in series with the respective first capacitor between the output node and a reference voltage source, and further comprises a second transistor coupled in series with the respective second capacitor between the output node and the reference voltage source, each transistor having a control terminal coupled to receive the corresponding phase shift control signal.

31. (Original) The data output circuit of claim 30 wherein the first transistor comprises an NMOS transistor and the second transistor comprises a PMOS transistor.

32. (Withdrawn) The data output circuit of claim 25 wherein the phase shift circuit comprises:

an input circuit adapted to receive the input clock signal and being operable to develop an output signal on an output responsive to the input clock signal;

an output circuit having an input coupled to a charging node and being operable to develop the phase shifted clock signal responsive to a charging signal on the charging node reaching a threshold value; and

a plurality of switching circuits coupled in series between the output of the input circuit and the charging node; each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the phase shift control signal having a first state to provide a first delay element and operable responsive to the phase shift control signal having a second state to provide a second delay element, the combination of first and second delay elements coupled in series controlling a rate at which the charging signal reaches the threshold value.

33. (Withdrawn) The data output circuit of claim 32 wherein the input and output circuits each comprise an inverter.

34. (Withdrawn) The data output circuit of claim 32 wherein each first delay element comprises a resistor and each second delay element comprises a transistor having signal terminals coupled in parallel with the corresponding resistor and having a control terminal coupled to receive the corresponding phase shift control signal.

35. (Withdrawn) The data output circuit of claim 34 wherein each transistor comprises a NMOS transistor.

36. (Withdrawn) The data output circuit of claim 25 wherein the phase shift circuit comprises:

an input circuit adapted to receive the input clock signal and including a ground node, the input circuit operable to develop the phase shifted clock signal responsive to the input clock signal, the phase shift of the phase shifted clock signal being a function of a supply current provided to the supply node; and

a plurality of switching circuits coupled in parallel between a ground voltage source and the ground node, each switching circuit coupled to the logic circuit to receive a respective one of the phase shift control signals and operable responsive to the phase shift control signal having a first state to provide a first current to the supply node and operable responsive to the phase shift control signal having a second state to provide a second current to the ground node, the combination of first and second currents from the plurality of switching circuits controlling the sink current provided to the ground node.

37. (Withdrawn) The data output circuit of claim 36 wherein each switching circuit comprises a transistor having signal terminals coupled between the ground voltage source and the ground node, and having a control terminal coupled to receive the corresponding phase shift control signal, and one switching circuit comprises a transistor having signal terminals coupled between the ground voltage source and the ground node and having a control terminal adapted to receive a bias voltage.

38. (Withdrawn) The data output circuit of claim 37 wherein each transistor comprises a NMOS transistor.

39. (Withdrawn) The data output circuit of claim 36 wherein the input circuit comprises a first inverter coupled to receive the input clock signal and including the ground node, and a second inverter coupled in series with the first inverter and operable to develop the delayed clock signal responsive to an output signal from first inverter.

40. (Previously presented) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a clock synchronization circuit adapted to receive an input clock and coupled to the read/write circuit to receive current data signals and respective future data signals, the clock synchronization circuit operable to generate a phase shifted clock signal in response to the input clock signal with the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and future data signals, the phase shifted clock signal being applied to data drivers in the read/write circuit to clock data onto the data bus.

41. (Currently amended) The memory device of claim 40 wherein the memory device comprises a ~~DDR SDRAM~~ double data rate synchronous dynamic random access memory.

42. (Previously presented) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a clock synchronization circuit adapted to receive an input clock and coupled to the read/write circuit to receive current data signals and respective future data signals, the clock synchronization circuit operable to generate a phase shifted clock signal in response to the input clock signal with the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and future data signals, the phase shifted clock signal being applied to data drivers in the read/write circuit to clock data onto the data bus.

43. (Currently amended) The computer system of claim 42 wherein the memory device comprises a ~~DDR SDRAM~~ double data rate synchronous dynamic random access memory.

44. (Previously presented) A method of providing data signals out of an integrated circuit in synchronism with a clock signal applied to the integrated circuit, the method comprising:

detecting a respective first logic state of each data signal;

detecting a respective second logic state of each data signal;

determining an output delay from the detected respective first and second logic states; and

adjusting a delay interval relative to a transition of the clock signal based on the determination; and

outputting the data signals having the second logic state from the integrated circuit in response to the adjusted delay interval.

45. (Previously presented) The method of claim 44 wherein the respective first logic state of each data signal comprises a current logic state and wherein the respective second logic state of each data signal comprises an upcoming logic state of the data signal.

46. (Previously presented) The method of claim 44 wherein determining an output delay from the detected respective first and second logic states comprises adding a first delay increment to the output delay for each corresponding pair of detected respective first and second logic states of each data signal where the detected respective first and second logic states are equal, and adding a second delay increment to the output delay for each corresponding pair of detected respective first and second logic states of each data signal where the detected respective first and second logic states are unequal.

47. (Original) The method of claim 46 wherein the first delay increment is greater than the second delay increment.

48. (Previously presented) A method of delaying data signals relative to a clock signal, comprising:

detecting a respective current logic state of each data signal;

detecting a respective future logic state of each data signal;

determining an output delay having a value that is a function of the detected respective current and future logic states for each data signal; and

delaying the data signals having the future logic state by the determined output delay relative to the clock signal.

49. (Previously presented) The method of claim 48 wherein determining the output delay comprises adding a first delay increment to the output delay for each corresponding pair of respective current and future logic states of each data signal where the detected respective current and future logic states are equal, and adding a second delay increment to the output delay for each corresponding pair of respective current and future logic states of each data signal where the detected respective current and future logic states are unequal.

50. (Original) The method of claim 49 wherein the first delay increment is greater than the second delay increment.

51. (Previously presented) A method of providing data signals out of an integrated circuit, the method comprising:

detecting respective current and future logic states for each data signal, each data signal having the respective current logic state having a phase shift relative to a clock signal;

adjusting the value of the phase shift in response to the detected respective current and future logic states; and

outputting the respective future logic state for each data signal, with each data signal having the respective future logic state being phase shifted by the adjusted value of the phase shift.

52. (Original) The method of claim 51 wherein adjusting the value of the phase shift in response to the detected current and future logic states comprises adjusting the value of the phase shift as a function of the number of data signals for which the values of the current and future logic states are equal and adjusting the value of the phase shift as a function of the number of data signals for which the current and future logic states are unequal.

53. (Original) The method of claim 52 wherein adjusting the value of the phase shift as a function of the number of data signals for which the values of the current and future logic states are unequal comprises decreasing a delay for each data signal for which the values of the current and future logic states are unequal.

54. (Original) The method of claim 53 wherein adjusting the value of the phase shift as a function of the number of data signals for which the values of the current and future logic states are equal comprises increasing a delay for each data signal for which the values of the current and future logic states are equal.

55. (Original) The method of claim 52 wherein adjusting the value of the phase shift as function of the number of data signals for which the values of the current and future logic states are unequal comprises adding a first delay increment to the phase shift for each such data signal, and wherein adjusting the value of the phase shift as function of the number of data signals for which the values of the current and future logic states are equal comprises adding a second delay increment to the phase shift for each such data signal.

56. (Original) The method of claim 55 wherein the first delay increment is less than the second delay increment.

57. (Previously presented) A method of providing data signals out of an integrated circuit in synchronism with a clock signal applied to the integrated circuit, the method comprising:

detecting a respective first logic state of each data signal;

detecting a respective second logic state of each data signal;

determining a respective output delay for each data signal from the corresponding detected respective first and second logic states; and

for each data signal, outputting the data signal having the second logic state in accordance with the determination of the respective output delay for each data signal from the integrated circuit.

58. (Previously presented) The method of claim 57 wherein the respective first logic state of each data signal comprises a current logic state and wherein the respective second logic state of each data signal comprises an upcoming logic state of the corresponding data signal.

59. (Previously presented) The method of claim 58 wherein determining a respective output delay from the detected respective first and second logic states comprises:

for each data signal,

defining a group of data signals associated with the data signal;

comparing the current and future logic states of the data signals in the group of data signals;

adjusting the output delay of the data signal as a function of the current and future logic states of the data signals in the group of data signals.

60. (Previously presented) The method of claim 59 wherein each group of data signals includes four data signals.

61. (Previously presented) The method of claim 60 wherein adjusting the output delay of the data signal as a function of the current and future logic states of the data signals in the group comprises adjusting the output delay to a first value when the current and future logic states of all data signals in the group are equal, adjusting the output delay to a second value when the current and future logic states of one data signal in the group is changing, adjusting the output delay to a third value when the current and future logic states of two data signals in the group are changing, and adjusting the output delay to a fourth value when the current and future logic states of more than two data signals in the group are changing.

62. (Original) The method of claim 61 wherein the first value is greater then the second value which is greater than the third value which is greater than the fourth value.

63. (Currently amended) A method of delaying data signals relative to a clock signal, comprising:

detecting a respective future logic state of each data signal;

defining a respective group of data signals associated with each data signal;

comparing respective current and corresponding respective future logic states of the data signals in the group;

determining an output delay for ~~the~~ each data signal~~s~~, the output delay of any one signal having a value that is a function of the detected respective future and current logic states of the corresponding data signals in its ~~the~~ associated group; and

delaying each data signal having the future logic state by the determined output delay relative to the clock signal.

64. (Previously presented) The method of claim 63 wherein each group comprises data signals being output from data terminals physically adjacent a data terminal from which the data signal is output.

65. (Original) The method of claim 63 wherein each group comprises data signals sharing a common voltage supply source.

66-74. (Cancelled)